Amendments to the Figures:

Please amend Figure 1 as indicated on the attached copy in the appendix by adding the legend –Prior Art--

REMARKS

Dear Sir:

This is a Response to the Office Action in the above referenced application mailed on January 12, 2005, and for which a 3-month extension is hereby requested. The Office Action rejected a number of claims under 35 U.S.C. 112, second paragraph. All of these rejections have been attended to, either in the appropriate claim itself or in claims into which they have been incorporated, in order to conform to the comments of the Office Action.

All of the pending claims were rejected under either 35 U.S.C. 102 or 103 based on a variety of references. Although all of the previously pending claims are believed allowable, several have been cancelled in order to more clearly focus the response below. The rejections of the remaining pending claims are discussed below under the appropriate heading. The non-elected claims have also been cancelled.

The Office Action also objected to Figure 1 due to lack of a "Prior Art" legend. This has now been added.

Claims 3-12

Claim 3 has been rewritten in independent form by incorporating the underlying limitations of original claims 1 and 2. Claims 4 and 6-12 have had their dependence changed to claim 3 so that all of claims 4-12 have claim 3 as their base claim.

The Office Action rejected claim 3 under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al.. It is respectfully submitted that this rejection is in error.

More specifically, claim 3 recites the limitation of "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*", where the emphasis has been added. With respect to this limitation, the Office Action states "Peyret further discloses that the mass storage is a flash memory (See Column 4 lines 63-67) which is a non-linear memory. Thus, the mass storage interface is inherently a non-linear interface." Peyret does disclose a flash memory, but otherwise the Office Action is making improper and incorrect assumptions. In particular, the term "flash" in "flash memory" refers to the manner in which the memory is *erased*, namely that cells are erased in groups (an erase block), and not to how

it is *accessed*. In particular, in its discussion of Figure 3 beginning on line 1 of column 6 where Peyret discusses the memory of a smart card and its being organized into an operating system layer, this would be indicative of a random access memory structure, rather than a non-linear interface structure. This distinction is structure is discussed in the present application as presented at, for example, the last two sentences of paragraph [0015] or paragraph [0032]. As far as can be determined, Peyret neither teaches nor suggests "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*".

Concerning the limitation of "a card bus whereby the processing unit, the interface and the program storage memory are connected", the Office Action references Figure 1 of Peyret. Figure 1 of Peyret shows CPU 22 connected to I/O 32 on one side, while on the *opposite* side on a *different* connection CPU 22 connects to the memory 24. Peyret does not disclose "***a card bus*** whereby the processing unit, the interface and the program storage memory are connected". As the added emphasis indicates, Peyret does not disclose that the elements that the Office Action identifies as the "processing unit", the "interface" and the "program storage memory" are connected along the *same* card bus; rather, distinct buses are indicated between the "processing unit" and the "interface" and between the "processing unit" and the "program storage memory".

As for the limitation of "a mass storage memory including a program memory portion storing at least one additional operating sequence", the Office Action cites Figure 1 and column 5, lines 7-11. The cited location does refer the storing of applets in NVM 30. (It should also be noted that these are applets, which specifically are applications of quite limited size.) However, the structure Peyret is that of a Smart Card, which, as discussed at paragraph [0010] of the present application, lacks "a mass storage memory". As far as can be determined, Peyret neither teaches nor suggests the inclusion of a mass storage memory: the discussion in terms of applets rather suggests the opposite. Thus, there is not disclosure of "a *mass storage memory* including a program memory portion storing at least one additional operating sequence", where the emphasis is added.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 3 and dependent claims 4-12 under U.S.C. 102(b) as anticipated by Peyret is not well founded and should be withdrawn.

Each dependent claims 4-12 is believed further allowable for the various additional

limitations which the recite; however, in order to reduce the length of an already complex response, the further allowability of these dependent claims will not be discussed further at this time.

Claims 15-25

Claim 15 has been rewritten in independent form by incorporating the underlying limitations of original claims 13 and 14. Claims 16, 17 and 22-25 have had their dependence changed to claim 15 so that all of claims 16-25 have claim 15 as their base claim.

The Office Action rejected claim 15 under 35 U.S.C. 102(b) as being unpatentable over US patent number 5,923,884 of Peyret et al.. It is respectfully submitted that this rejection is in error.

More specifically, claim 15 recites the limitation of "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*", where the emphasis has been added. With respect to this limitation, the Office Action states "Peyret further discloses that the mass storage is a flash memory (See Column 4 lines 63-67) which is a non-linear memory. Thus, the mass storage interface is inherently a non-linear interface." Peyret does disclose a flash memory, but otherwise the Office Action is making improper and incorrect assumptions. In particular, the term "flash" in "flash memory" refers to the manner in which the memory is *erased*, namely that cells are erased in groups (an erase block), and not to how it is *accessed*. In particular, in its discussion of Figure 3 beginning on line 1 of column 6 where Peyret discusses the memory of a smart card and its being organized into an operating system layer, this would be indicative of a random access memory structure, rather than a non-linear interface structure. This distinction is structure is discussed in the present application as presented at, for example, the last two sentences of paragraph [0015] or paragraph [0032]. As far as can be determined, Peyret neither teaches nor suggests "a mass storage interface by which the mass storage memory is connected to the card bus, *wherein the mass storage interface is a non-linear interface*".

Concerning the limitation of "a card bus whereby the processing unit, the interface and the program storage memory are connected", the Office Action references Figure 1 of Peyret. Figure 1 of Peyret shows CPU 22 connected to I/O 32 on one side, while on the *opposite* side on a *different* connection CPU 22 connects to the memory 24. Peyret does not disclose "***a card bus*** whereby the processing unit, the interface and the program storage memory are connected". As the added

emphasis indicates, Peyret does not disclose that the elements that the Office Action identifies as the "processing unit", the "interface" and the "program storage memory" are connected along the *same* card bus; rather, distinct buses are indicated between the "processing unit" and the "interface" and between the "processing unit" and the "program storage memory".

As for the limitation of "a mass storage memory", the Office Action cites Figures 1 and 4, element 30, and column 5, lines 13-35. Peyret does disclose memory 24; however, the structure Peyret is that of a Smart Card, which, as discussed at paragraph [0010] of the present application, lacks "a mass storage memory". As far as can be determined, Peyret neither teaches nor suggests the inclusion of a mass storage memory: the uses described for the memory rather require only a limited memory capability. Thus, it is respectfully submitted that there is no disclosure of "a mass storage memory".

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 15 and dependent claims 16-25 under U.S.C. 102(b) as anticipated by Peyret is not well founded and should be withdrawn.

Each dependent claims 16-25 is believed further allowable for the various additional limitations which the recite; however, in order to reduce the length of an already complex response, the further allowability of these dependent claims will not be discussed further at this time.

Claims 27-35

Claim 33 has been rewritten in independent form by incorporating the underlying limitations of original claim 26. Further, it has been amended to read "wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory", where the underlined portion was added beyond what was in the combined limitations of original claims 33 and 26. Claims 27-29, 31, 32, 34 and 35 have had their dependence changed to claim 33 so that all of claims 27-32, 34, and 35 have claim 33 as their base claim.

The Office Action rejected claim 33 under 35 U.S.C. 103(a) as being unpatentable over US patent number 6,047,342 of Depew et al. and US patent number 6,097,618 of Jenne, where the Jenne reference is cited to provide the non-volatile mass storage memory that the Office Action admits to be missing in Depew. It is respectfully submitted that this rejection is in error for a number of

reasons.

More specifically, the first step of claim 33 (as amended) reads:

> providing an add-on card with a processing unit and a non-volatile mass storage memory, wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory

The Office Action identifies the "non-volatile mass storage memory" with element 354 of Depew. This is respectfully submitted to be in error. Depew provides no disclosure of element 354 having any mass storage capability or being anything more than a standard RAM for use in the operation of the processor. Specifically, as far as can be determined, the only function assigned to RAM 354 is to serve as a buffer for the data in transit between the host and DVD Decoder 350. Consequently, Depew has no disclosure of "providing an add-on card with ... a non-volatile mass storage memory.

This first step of claim 33 also states that "a plurality of applications are stored on the add-on card, *with one or more of said applications stored in the non-volatile mass storage memory*", where the emphasis has been added. Depew has no disclosure of storing an application in what the Office Action identifies with the non-volatile mass storage memory", namely element 354, whose only disclosed function is to serve as a buffer, as is noted above. (The only related sort of memory function disclosed in Depew is for ROM 360 at column 7, lines 25-28, which describes that "ROM 360 contains instructions used to initialize the functions of data flow control ...".)

Further, as Depew has no disclosure of "a mass storage memory", there is no disclosure of "processing data stored in the mass storage memory": the only stored data processed is from the buffer memory of RAM 354.

Also, it is respectfully submitted that it would not be obvious to combine Depew with Jenne as described in the Office Action in order to replace Depew's RAM 354 with a non-volatile RAM of Jenne. The only function disclosed for RAM 354 in Depew is as a buffer for data being transferred between the host and DVD decoder 350, in which case there is no motivation to "provide fault tolerance by preventing a loss of information stored in the memory when power is removed or temporarily lost", as stated in the Office Action: If the card was removed or power lost, the processing would be started over and a buffer would need to be reloaded whether it were non-volatile or not. And as for any advantage due to storing an application in a non-volatile memory, first, as noted above, Depew has no disclose of storing an application in what the Office Action identifies as

the mass storage memory in Depew (354); secondly, where Depew has any disclosure of storing an application (or portions thereof) is already non-volatile, namely in ROM.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 33, along with its dependent claims 27-32, 34, and 35, under 35 U.S.C. 103(a) as being unpatentable over Depew Jenne is not well founded and should be withdrawn.

Each dependent claims 27-32, 34, and 35 is believed further allowable for the various additional limitations which the recite. However, in order to reduce the length of an already complex response, the further allowability of these dependent claims will not be discussed further at this time.

Claims 37-42

Claim 41 is similar to claim 33, except that instead of processing data stored in the non-volatile mass storage memory and providing it to the host, it processes data from the host and stores it in the non-volatile mass storage memory. Claim 41 was rejected for much the same reasons as claim 33 and is believed allowable more much the same reasons.

Claim 41 has been rewritten in independent form by incorporating the underlying limitations of original claim 36. Further, it has been amended to read "wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory", where the underlined portion was added beyond what was in the combined limitations of original claims 41 and 36. Claims 37, 38, 40, and 42- have had their dependence changed to claim 41 so that all of claims 37-40 and 42 have claim 41 as their base claim.

The Office Action rejected claim 41 under 35 U.S.C. 103(a) as being unpatentable over US patent number 6,047,342 of Depew et al. and US patent number 6,097,618 of Jenne, where the Jenne reference is cited to provide the non-volatile mass storage memory that the Office Action admits to be missing in Depew. It is respectfully submitted that this rejection is in error for a number of reasons.

More specifically, the first step of claim 41 (as amended) reads:

> providing an add-on card with a processing unit and a non-volatile mass storage memory, wherein a plurality of applications are stored on the add-on card, with one or more of said applications stored in the non-volatile mass storage memory

The Office Action identifies the "non-volatile mass storage memory" with element 354 of Depew.

This is respectfully submitted to be in error. Depew provides no disclosure of element 354 having any mass storage capability or being anything more than a standard RAM for use in the operation of the processor. Specifically, as far as can be determined, the only function assigned to RAM 354 is to serve as a buffer for the data in transit between the host and DVD Decoder 350. Consequently, Depew has no disclosure of "providing an add-on card with ... a non-volatile mass storage memory.

This first step of claim 41 also states that "a plurality of applications are stored on the add-on card, *with one or more of said applications stored in the non-volatile mass storage memory*", where the emphasis has been added. Depew has no disclosure of storing an application in what the Office Action identifies with the non-volatile mass storage memory", namely element 354, whose only disclosed function is to serve as a buffer, as is noted above. (The only related sort of memory function disclosed in Depew is for ROM 360 at column 7, lines 25-28, which describes that "ROM 360 contains instructions used to initialize the functions of data flow control ...".)

Further, as Depew has no disclosure of "a mass storage memory", there is no disclosure of "storing the processed data in the mass storage memory": the only stored data processed is from the buffer memory of RAM 354.

Also, it is respectfully submitted that it would not be obvious to combine Depew with Jenne as described in the Office Action in order to replace Depew's RAM 354 with a non-volatile RAM of Jenne. The only function disclosed for RAM 354 in Depew is as a buffer for data being transferred between the host and DVD decoder 350, in which case there is no motivation to "provide fault tolerance by preventing a loss of information stored in the memory when power is removed or temporarily lost", as stated in the Office Action: If the card was removed or power lost, the processing would be started over and a buffer would need to be reloaded whether it were non-volatile or not. And as for any advantage due to storing an application in a non-volatile memory, first, as noted above, Depew has no disclose of storing an application in what the Office Action identifies as the mass storage memory in Depew (354); secondly, where Depew has any disclosure of storing an application (or portions thereof) is already non-volatile, namely in ROM.

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 41, along with its dependent claims 37-40 and 42, under 35 U.S.C. 103(a) as being unpatentable over Depew Jenne is not well founded and should be withdrawn.

Each dependent claims 37-40 and 42 is believed further allowable for the various additional limitations which the recite. However, in order to reduce the length of an already complex response, the further allowability of these dependent claims will not be discussed further at this time.

Claims 43-50

The Office Action rejected independent claim 43 under U.S.C. 102(b) as anticipated by US patent number 5,987,155 of Dunn et al. and US patent 6,038,551 of Barlow et al.. It is respectfully submitted that these rejections are in error.

More specifically, with respect to Dunn, claim 43 includes the step of step of "providing an add-on card including ... a non-volatile mass storage memory, wherein the mass storage memory includes a program memory portion in which are stored a plurality of applications", for which the Office Action refers to column 3, lines 22-28 of Dunn; however, this portion of Dunn is only giving a general description of a Smart Card as it is found in the prior art ("The Smart card comprises a microprocessor, non-volatile storage and random access memory (RAM) all on a small portable card") similar to that found in paragraph [0010] in the present application. Although such cards have some non-volatile storage, they lack "a non-volatile mass storage memory"; further, although they may have some program storage, this is not in the "non-volatile mass storage memory". Consequently, they explicitly do not possess a "mass storage memory include[ing] a program memory portion in which are stored a plurality of applications". These are not features found in the prior art smart card and they are not found in any other of Dunn's teachings. (Also, in the location cited by the Office Action, there is no disclosure of "causing one of the applications to be selected": Although at column 7, lines 38-41 a number of function are disclosed, these are all performed on the host computer, as is clear from the preceding sentence (col. 7, lns. 35-37).

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 43 and dependent claims 44-50 under U.S.C. 102(b) as anticipated by Dunn is not well founded and should be withdrawn.

As for Barlow, with respect to the step of "providing an add-on card including ... a non-volatile mass storage memory, wherein the mass storage memory includes a program memory portion in which are stored a plurality of applications", the Office Action refers to Figure 3, element

number 54; however, this element is ROM, not a "mass storage memory" since, as the user cannot write to ROM, they cannot store data at all in ROM 54, much less have it function as a "mass storage memory". Further, there is no disclosure of storing "a plurality of applications" in ROM 54, but only CRYPTOGRAPHIC PROGRAM 66. (Also, at the cited location, it is not clear that Barlow discloses "causing one of the applications to be selected" as there is only the application of a "cryptographic function".)

Consequently, for any of these reasons, it is respectfully submitted that a rejection of claim 43 and dependent claims 44-50 under U.S.C. 102(b) as anticipated by Barlow is not well founded and should be withdrawn.

Each dependent claims 44-50 is believed further allowable for the various additional limitations which the recite. For example, claim 44, which has the limitation of "wherein the selected application is an application which the host lacks", is also rejected under U.S.C. 102(b) as anticipated Barlow; however, as is clear beginning from line 7 of Barlow's Abstract, not only is the application is application ***not*** lacking in the host, but is rather *dependent* upon the host. Similarly, for its rejection of claim 45 under U.S.C. 102(b) as anticipated Barlow, the Office Action refers to column 16, lines 63-66; however, this sentence only refers to a standard process of sending a data stream, not of "continuous media", such as is presented in the present application (see, for example, paragraph [0036], next to last sentence). But, in order to reduce the length of an already complex response, the further allowability of these dependent claims will not be discussed further at this time.

Claims 54 and 55

The Office Action rejected claims 54 and 55 under U.S.C. 102(b) as anticipated by US patent number 6,047,342 of Depew et al.. It is respectfully submitted that these rejections are in error.

The last element of claim 54 is:

> processing data according to the selected application, wherein said processing is performed by the card's processing unit and the host processing system together on an application level.

A particular embodiment of this step is provided in claim 55:

> wherein said processing comprises executing a plurality of tasks, and wherein at least one of the tasks is executed by the host processing system and at least one of the tasks is allocated by the host to be executed by the card's processing unit.

It is respectfully submitted that not only are these elements not found in Depew, but that Depew rather teaches to the contrary.

More specifically, with respect this element of claims 54 and 55 the Office Action cites column 6, lines 20-37 and column 7, lines 43-54. However, beginning at line 25 of column 6, Depew states:

> CPU 310 [of computer system 300], however, *does not decompress the compressed DVD data or perform any other significant amount of processing. CPU 310 is relegated to the task of simply managing the flow of data* from DVD drive 316 to PC processing card 340.

As the added emphasis indicates, this does ***not*** describe that the "processing is performed by the card's processing unit and the host processing system together on an application level", as stated in the claims; but, rather, Depew explicitly states that host processing system does not take part in the processing itself at the application level and only oversees the flow of data on and off the card.

Consequently, it is respectfully submitted that a rejection of claims 54 and 55 under U.S.C. 102(b) as anticipated by Depew is not well founded and should be withdrawn.

New Claims

New claims 63 and 64 have been added. These are dependent claims and differ from each other only in respectively having claims 33 and 41 as their base claim. Both add the further limitation of "wherein the non-volatile mass storage memory accessed through a non-linear interface." Consequently, these claims are believed further allowable for reasons similar to those discussed above with respect to claims 3 and 15. Further, it is noted that claims 33 and 41 were rejected under 35 U.S.C. 103(a) as being unpatentable over Depew and Jenne, where the Jenne reference is cited to provide the non-volatile mass storage memory that the Office Action admits to be missing in Depew. However, as is clear at the cited location of column 2, lines 20-34, of Jenne, Jenne's teachings are directed to a non-volatile *random access* non-volatile memory, which is thus teaching away from the sort of non-linear interface for a memory in which an application is stored, in the present application as presented at, for example, the last two sentences of paragraph [0015] or paragraph [0032].

Notice of References Cited (PTO-892)

The Office Action cited US patent number 5,987,155 of Dunn et al.; however, this reference was not listed on the form PTO-892 that accompanied the Office Action. Applicants request that a Notice of References Cited (PTO-892) that includes this reference be supplied in order to kept track in the record that this reference was considered.

Conclusion

For each of the reasons given above, it is therefore respectfully submitted that the each of the rejections of each of the pending is improper and should be withdrawn. Reconsideration of these claims, along with consideration of new claims 63 and 64, and an early indication of the allowance of the present application are earnestly solicited.

Respectfully submitted,

Gerald P. Parsons — July 12, 2005

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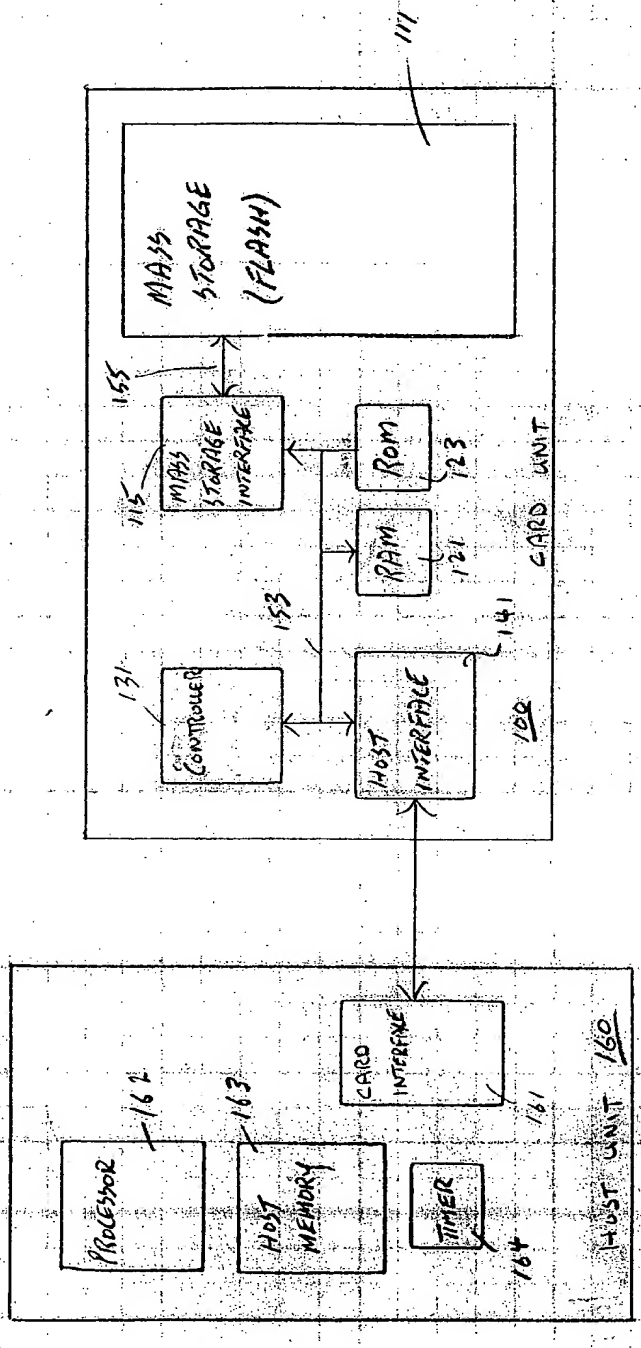

FIGURE 1
(Prior Art)

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